Full field lithographical verification using scanner and mask intrafield fingerprint

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ABSTRACT

Full chip verification has become a key component of the optical proximity correction (OPC) methodology over the last decade. Full field verification to catch cross-field effects based on scanner information is becoming increasingly important in lithography verification. Lithographic Manufacturing Check (LMC) performed with the Brion Tachyon engine, which is the industry reference tool, now provides the capability to predict wafer CD variations across the entire field through process windows. LMC is catching and reporting weak lithographic points having small process windows or excessive sensitivities to mask errors based on the simulation from models with ASML scanner specific parameters.

ASML scanner intra-field information such as dose, focus, flare, illuminator map, aberration data or mask bias map can be integrated into the LMC run to create an across-field verification and can improve the accuracy of the prediction at different field locations. In this study we compare such across-field LMC verification with a reference LMC without any scanner specific data.

Scanner information was loaded into the LMC model by using the Scanner Fingerprint File (SFF) functionality. Various across field LMC runs using scanner information have been performed and analysed to identify critical design hotspots or scanner drifts and compared with wafer measurement.

Full field Tachyon LMC results on 40nm Poly and 28nm Metal1 layer are presented. The goal is to investigate the impact of mask, lens aberrations, illuminator, dose and focus map. This investigation includes wafer validation of the methodology on identified critical hot spots.

Keywords: Lithographic verification, across field verification, intrafield fingerprint, SEM, Process Window analysis

1. INTRODUCTION

The main purpose of this paper is to study the pertinence of introducing process data during full field lithographical simulation by comparing simulation with wafer measurement. In fact with the diminution of Critical Dimensions (CD), litho process reaches the limit of resolution and new techniques (such as double patterning [1] and pixelated sources [2]) are required to overcome these limitations. Process control to decrease variability is becoming more and more important and challenging with these new techniques: for the 20nm node, the overall CDU budget allowed for the Gate CD is less than 1.9 nm (3σ) [3]. Based on these new challenges and specification, parallel development between process control and computational lithography/RET appears as a key way to reduce variability.

RET (Resolution Enhancement Techniques) goal is to ensure a good mask-to-silicon transfer which usually includes phase shifting mask, off-axis illumination and OPC. OPC is commonly used to compensate lithography process effects by modifying shapes on the mask using models which are able to predict printing at wafer level. Models are also used on Litho Manufacturing Check (LMC) to run a full field simulation and predict wafer CD across the field [4],[5]. The main goal is to highlight design regions with small process window and predict hotspots more accurately before ordering a mask.

Figure1 compares the traditional OPC/LMC flow and the proposed one. Currently OPC and LMC models are built for one particular process, one particular scanner (optical condition) and using an ideal mask. This methodology does not allow a dynamic link between process and models and no possibility to follow by simulation a non-ideal mask process or scanner behaviour. New flow developed to overcome these limitations (figure1) can be divided into 3 steps:

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- Step 1: Collect scanner information to integrate it into the Tachyon model engine. The procedure is to connect to LithoServer™, collect scanner files and generate a Scanner Fingerprint File (SFF) compiling all relevant scanner information. This file can then easily be transferred into the Tachyon models. The study was done with illuminator, aberrations and stray-light but also a dose and focus map (not loaded via SFF). Discrete measured CD provided by the mask shop were also used and fitted during mask preparation to generate a Mask Bias Map Verification (MBMV) [6].
- Step 2: Run LMC (or OPC) with this new process information. The focus of this paper was on the LMC check operation and hotspot evolution.
- Step 3: Adapt process condition using scanner knobs (DoseMapper™ [7],[8], Illuminator…) to take into consideration weak lithographic points highlighted by Tachyon LMC.

Brion recently developed a new tool which can tune scanner parameters based on the CD predictions from a specific litho condition. The tool called cPM (computational Pattern Matcher), can be used to set scanner parameters as shown in the figure 1. The cPM will however not be discussed in detail during this study.

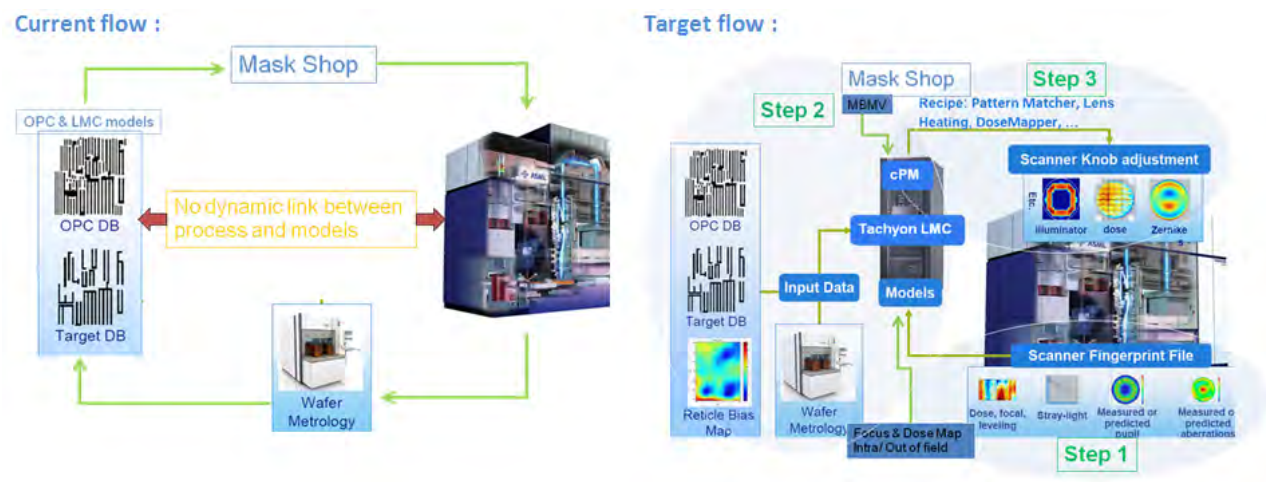

Figure 1 : Current OPC/LMC flow versus target flow

This method was tested on 40nm Poly and 28nm Metal1 with full field Tachyon lithographic simulation, results are presented hereafter. The goal is to investigate impact of mask, lens aberrations, illuminator, dose and focus map. This investigation includes wafer validation of the methodology on identified critical hotspots.

2. EXPERIMENT AND RESULTS

2.1 Experimental setup

Tachyon LMC is a software solution for RET verification that implements fast and accurate lithography simulation based on Brion Tachyon systems [4]. It compares the simulated wafer image with the design target to detect any RET layout error or deviations. Tachyon LMC is widely used for mask layout signoff. Tachyon LMC can predict the exact regions on a mask that are sensitive to process condition changes and are likely to create manufacturing weak spots on wafer that are sensitive to process condition changes (hotspots) [5]. In this paper, we used Tachyon LMC together with scanner information to enable hotspots identification across the full field.

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The study was carried out on 40nm Poly layer process using ASML XT:1700i scanner, and on 28nm Metal1 layer using ASML NXT:1950i scanner. Scanner fingerprints information was loaded into LMC using scanner fingerprint file (SFF) functionality. Similarly, mask bias map variation (MBMV), dose map and focus maps were loaded.

Various across field LMC runs with real scanner information were performed and compared to identify critical design hotspots. Tachyon LMC reports the defects which are outside the user defined tolerances for each process window condition.

Comparative analysis of new detected defects, hotspots count and evolution was conducted as well as exposure latitude and depth of focus (DOF) evolution. The latter has been performed using Tachyon cutline analysis tool. Results are presented in next section.

2.2 Results

2.2.1 40nm node Poly results

An intrafield / scanner characteristic integration with LMC study was done on a 40nm matrix product. That product consists of a 15 repeatable blocks (figure2), which is particularly interesting to perform an intrafield analysis.
That mask was exposed on an ASML XT:1700i. The scanner fingerprint file was then generated successfully with relevant information from the scanner (pupil map, aberration and straylight) and focus map and MBMV were collected.

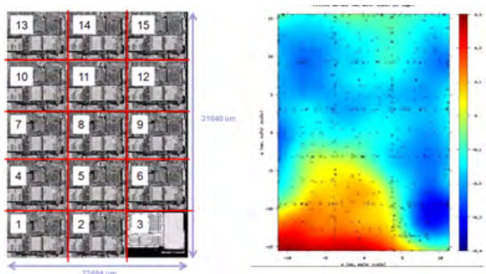

Figure 2 : 40nm Poly chip overview with associated mask bias map variation

4 full field LMC runs were performed full field (15 blocks merged).
- The first one being the reference without any intrafield or scanner fingerprint info (reference)
- The second with intrafield data coming from the mask shop via the mask bias map variation (MBMV).
- The third one with the scanner fingerprint file (SFF)
- The last run is done with intrafield defocus map (focus-map). This LMC run was performed via the Tachyon scripting LUA language where the PW conditions and detectors were re-defined.

Figure 3 illustrates one example of hotspot evolution as a function of process contribution and position in the field. On the specific example shown here the difference can go up to 3.5 nm.

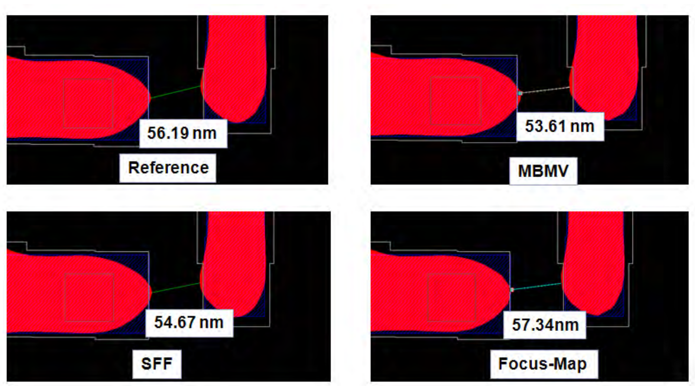

Figure 3: 40nm Poly same hotspot worst-case for each LMC run

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Finally, all the intrafield components were combined to better predict the impact on silicon. Hotspots were compared with wafer CD measurements through dose and focus (Focus Exposure Matrix : FEM) :

- Figure 4 below illustrates an example of hotspot simulated which matches wafer image. Hotspot was selected at process window edge to increase criticality. Comparing SEM pictures on 2 different blocks of the same field indicated that bridging is location dependant within the field. The MBMV LMC intrafield run showed the same trend: the bridging risk increases at the bottom of the field. The LMC run with SFF and with the focus map were not impacted by the location in the field: the simulation differences were less than 1 nm (which is within the measurement noise) whatever the defects and the location. Two hypotheses can be formulated: scanner intrafield parameters (illuminator on 5 slits positions, lens aberrations, focus variation) impact is limited or intrafield effects are negligible for model.

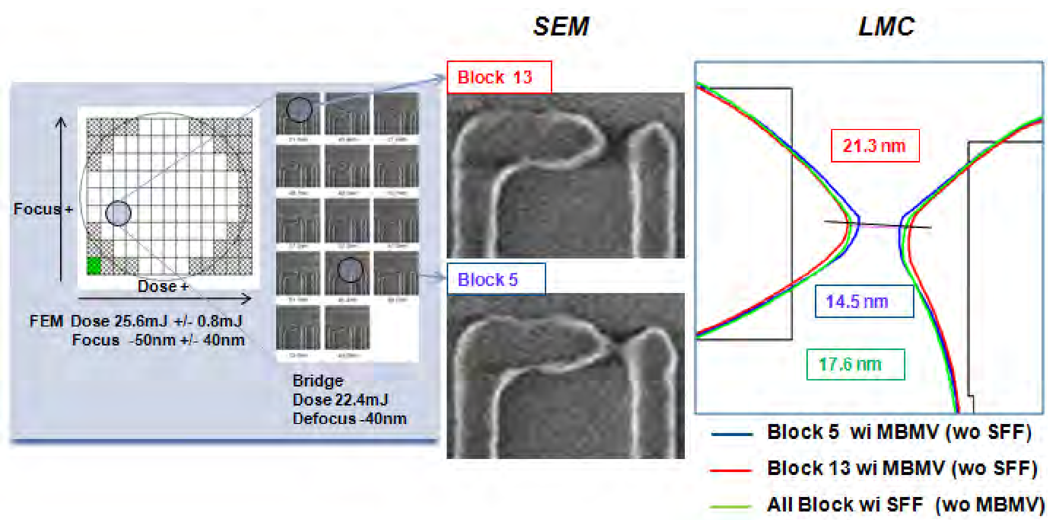

Figure 4 : Bridging SEM measure, MBMV LMC, SFF LMC intrafield comparison

- Scatter-bar printing is another example of good correlation between MBMV simulation wafer image as illustrated in Figure 5:

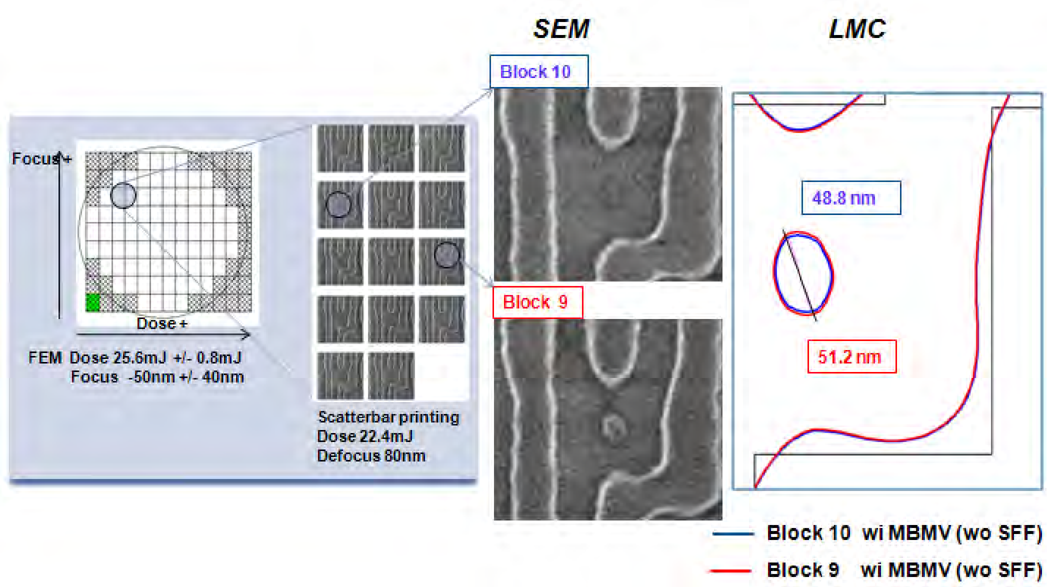

Figure 5 : ScatterBar printing SEM measurement, MBMV LMC comparison without SFF

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- The following example (figure 6) illustrates that few hotspot structures are not well predicted by MBMV simulations:

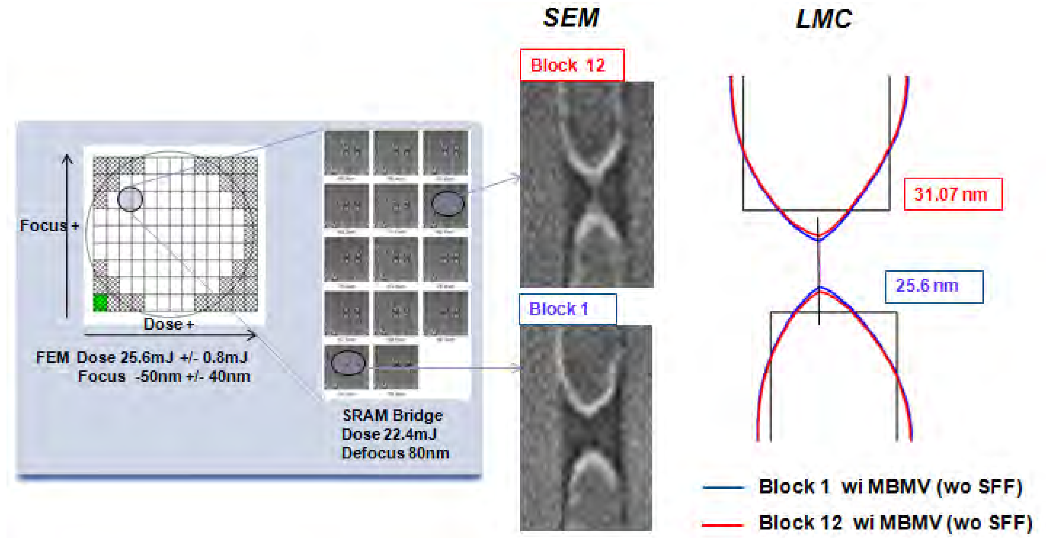

Figure 6 : SRAM bridging SEM measurement, MBMV LMC, comparison without SFF

This mismatch between measurement and simulations could be explained by the fact that other intrafield/interfield effects are impacting this area (Flare, MSD…) or by the fact scumming is not well predicted with current model. It could be interesting to integrate those effects in follow-up studies. The mismatch could also be explained by an accuracy issue of the MBMV SEM sampling in this field area.

This initial study showed a good correlation between SEM and Tachyon simulations for most of the cases. The mask fingerprint was the major contributor to the intrafield CD variation, while the scanner intrafield fingerprint parameters did not show any significant impact.

2.2.2 28nm node Metal results

Similar work was done on a 28nm Metal product with 4 identical blocks distributed in the field (figure 7):

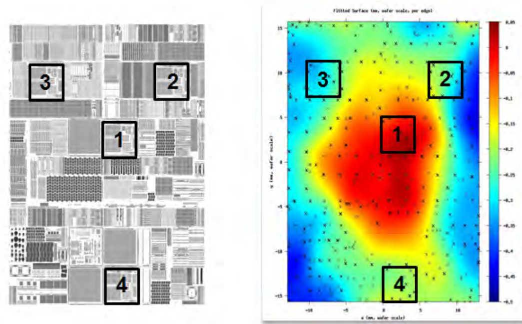

Figure 7 : 28nm Metal chip overview with associated mask bias map variation

Simulation was performed with various options such as MBMV, SFF, Dose Map and a combination of all. A wafer was exposed on an ASML NXT:1950i scanner through dose and focus. SEM images measurements were compared to simulation results. As 40nm Poly level, the major contribution on LMC is mask bias. SEM versus simulation comparison analysis was focus on this contribution. Figure 8 illustrates an example good correlation between LMC MBMV simulation and SEM measure for a bridging hotspot:

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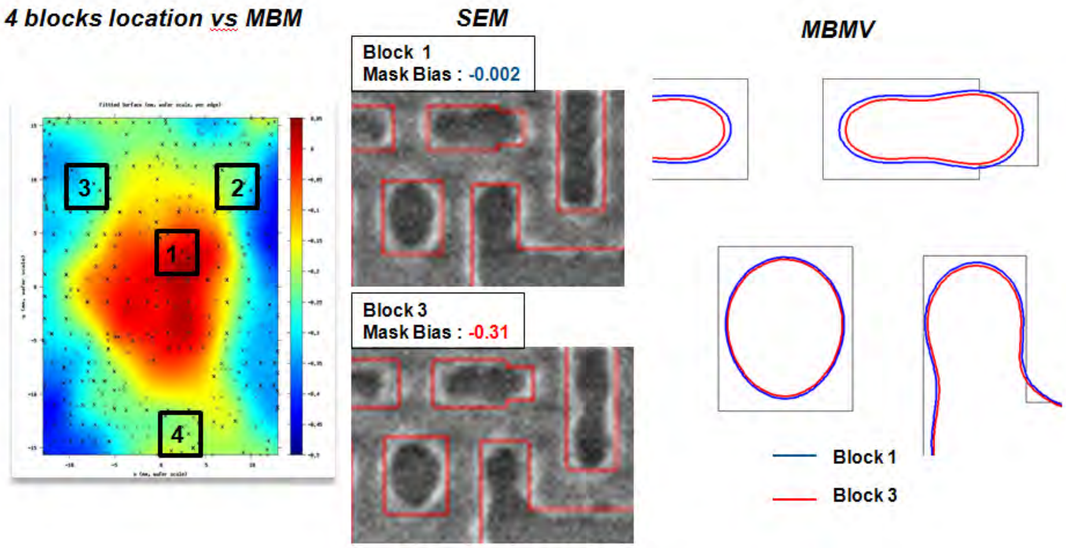

Figure 8 : 28nm Metal mask bias map, hotspot SEM measurement and LMC with MBMV

Based on this first analysis, most critical bridge and neck defects were measured full-map and compared with simulation using Tachyon LMC process window analysis (PWA) tool. We report the study on the necking and the bridging hotspot illustrated in figure 9.

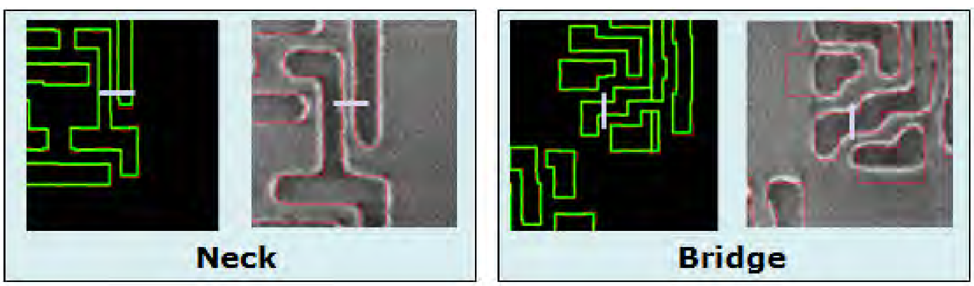

Figure 9 : 28nm Metal bridging and necking hotspot example

These defects were analyzed at 4 different intrafield locations by reporting the Process Windows (either simulated or measured). Individual process windows of specific defects are similar but due to an intrafield mask fingerprint in the center of the field (which met specification) the overlapping process window is significantly reduced (by at least 30%).

Figure 10 below clearly shows the impact of the mask fingerprint on the bridging hotspot, shifting down the process window for the center part of the mask (from the red PW for position 4 to the green PW for position 1). The dose at that center position is shifted by almost 2%. This offset results in a smaller overlapping process window, represented by the blue ellipse, which is reduced by more than 50% for that particular hotspot.

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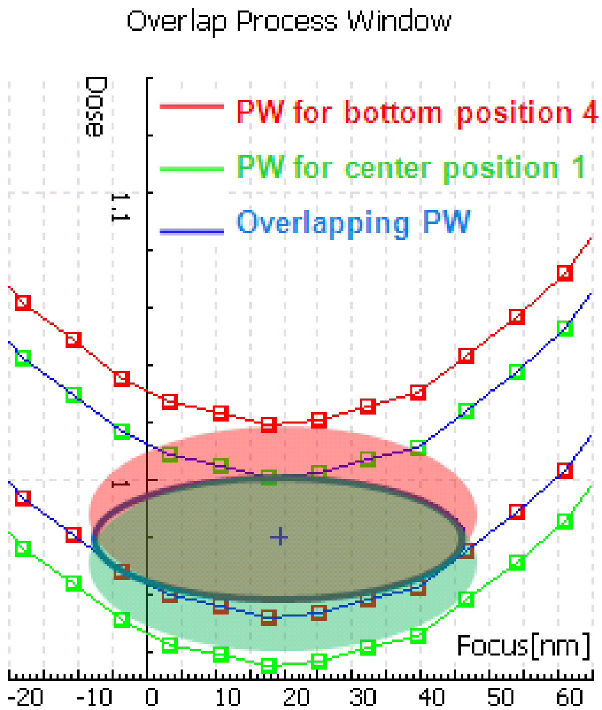

Figure 10 : Process windows for the bridge hotspot at position 1 and 4

2.2.3 28nm node Metal results : process window control and improvement

Next step in this study was to include dose map used by DoseMapper [7],[8], to correct the reticle fingerprint and compare its impact on simulation and SEM. The dose map (DOMA) used as input for the DoseMapper scanner recipe correction has been generated only using the reticle fingerprint (no etch or process fingerprint). This dose map can be easily loaded into Tachyon LMC using the LUA scripting language.

The figure of merit used here was the percentage improvement in overlapping Process Windows. The graphs below illustrate the evolution of the process windows calculated at +/-10% of 38 nm target CD for the bridge and +/-10% of 52 nm for the necking case.

Figure 12 compares, for the bridging hotspot, the simulated EL versus DOF with and without the dose map. Figure 11 reports the measurement data also with/without the dose map. Similar analysis was performed on Figure 13 and 14 for the necking hotspot.

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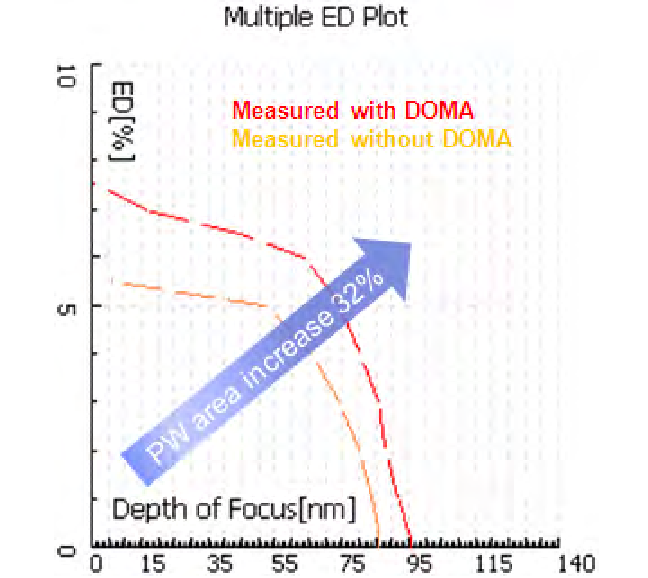

Figure 11 : Bridge hotspot, measured process windows with/without dose map

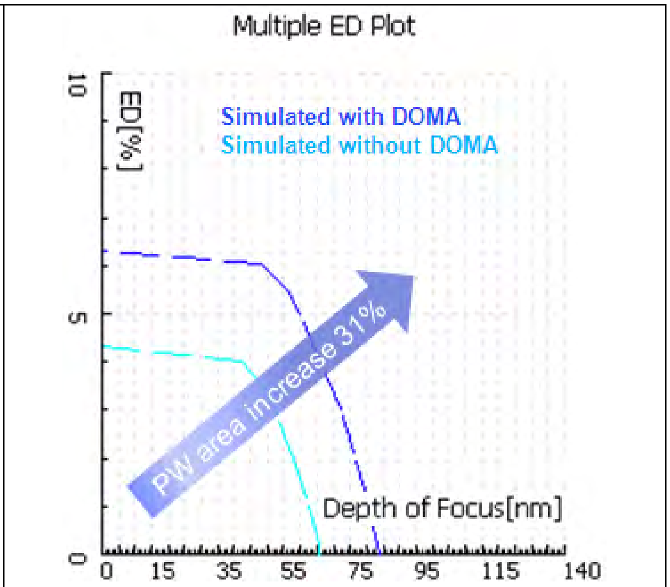

Figure 12 : Bridge, simulated process windows with/without dose map

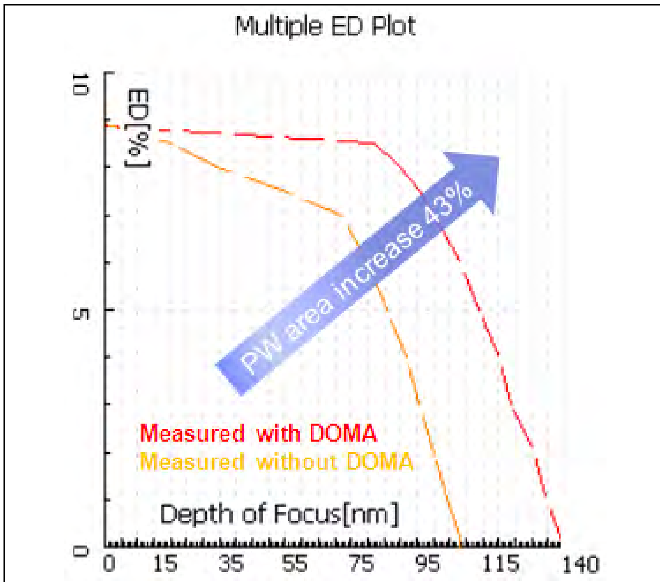

Figure 13 : Neck hotspot, measured process windows with/without dose map

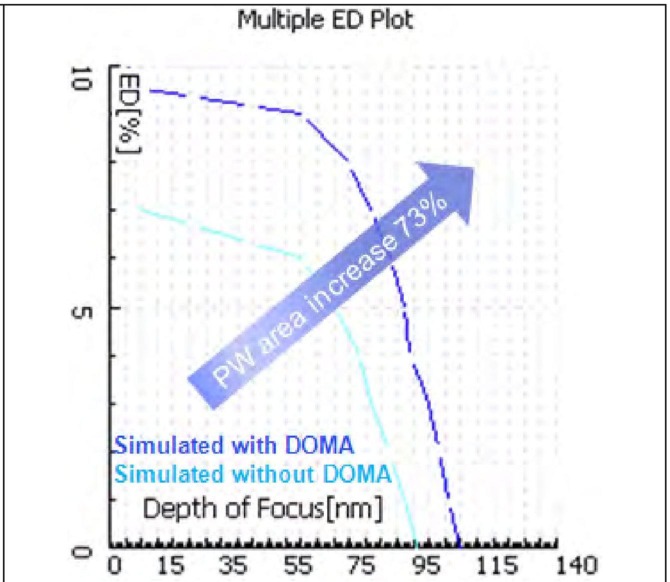

Figure 14 : Neck, simulated process windows with / without dose map

A strong correlation between simulations and measurements is observed. The offset present between simulation and wafer data can be explained by the measurement data quality. Significant PW enhancement is observed after entering dose map correction, which was confirmed by both simulation and measurement. Measured process window area improvement is over 30% for bridging case and 40% for necking limited cases. A similar trend was confirmed on all other types of hotspots.

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3. CONCLUSION

Tachyon LMC can carry out more accurate simulations with the input of intrafield information from the scanner or the mask. LMC runs with mask bias map variation, focus map and scanner fingerprint file were performed succesfully on 40 nm Poly layer and repeated on 28nm Metal level. Among all these effects, mask variation displayed the most significant impact on CD, while scanner intrafield variations are negligible. These results are consistent with wafer measurement data. It was found that considerable CD and PW improvement can be achieved by applying a dose map correction to compensate for a mask variation and that such correction is properly simulated.

Future analysis will focus on CDU to increase reliability and to collect more statistical information. Similar work will be done with other scanners contribution (Out-of-field straylight, laser…). An exploration will be also made on other scanner knobs such as flexray^{TM} and flexwave^{TM} (step 3 on figure 1), still on the goal to improve dynamic link between LMC and process control.

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